

FIG. 1

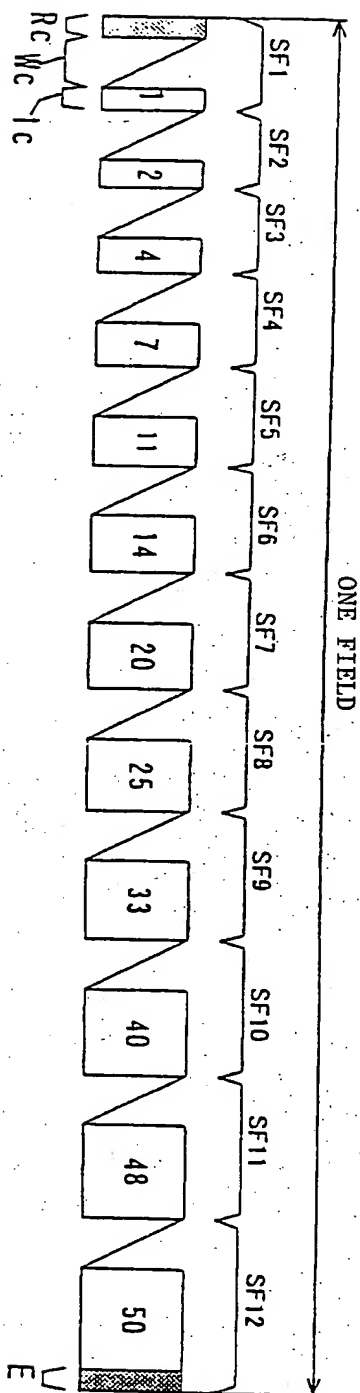


FIG. 2

● : SELECTIVE-ERASE DISCHARGE
○ : LIGHT EMISSION SF

GRADATION

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GRADATION	CONVERSION TABLE												LIGHT EMISSION DRIVE PATTERN	DISPLAY BRIGHTNESS	
	PDs	GD													
		1	2	3	4	5	6	7	8	9	10	11			12
1	0000	1	0	0	0	0	0	0	0	0	0	0	0	●	0
2	0001	0	1	0	0	0	0	0	0	0	0	0	0	○	1
3	0010	0	0	1	0	0	0	0	0	0	0	0	0	○	3
4	0011	0	0	0	1	0	0	0	0	0	0	0	0	○	7
5	0100	0	0	0	0	1	0	0	0	0	0	0	0	○	14
6	0101	0	0	0	0	0	1	0	0	0	0	0	0	○	25
7	0110	0	0	0	0	0	0	1	0	0	0	0	0	○	39
8	0111	0	0	0	0	0	0	0	1	0	0	0	0	○	59
9	1000	0	0	0	0	0	0	0	0	1	0	0	0	○	84
10	1001	0	0	0	0	0	0	0	0	0	1	0	0	○	117
11	1010	0	0	0	0	0	0	0	0	0	0	1	0	○	157
12	1011	0	0	0	0	0	0	0	0	0	0	0	1	○	205
13	1100	0	0	0	0	0	0	0	0	0	0	0	0	○	255

FIG. 3

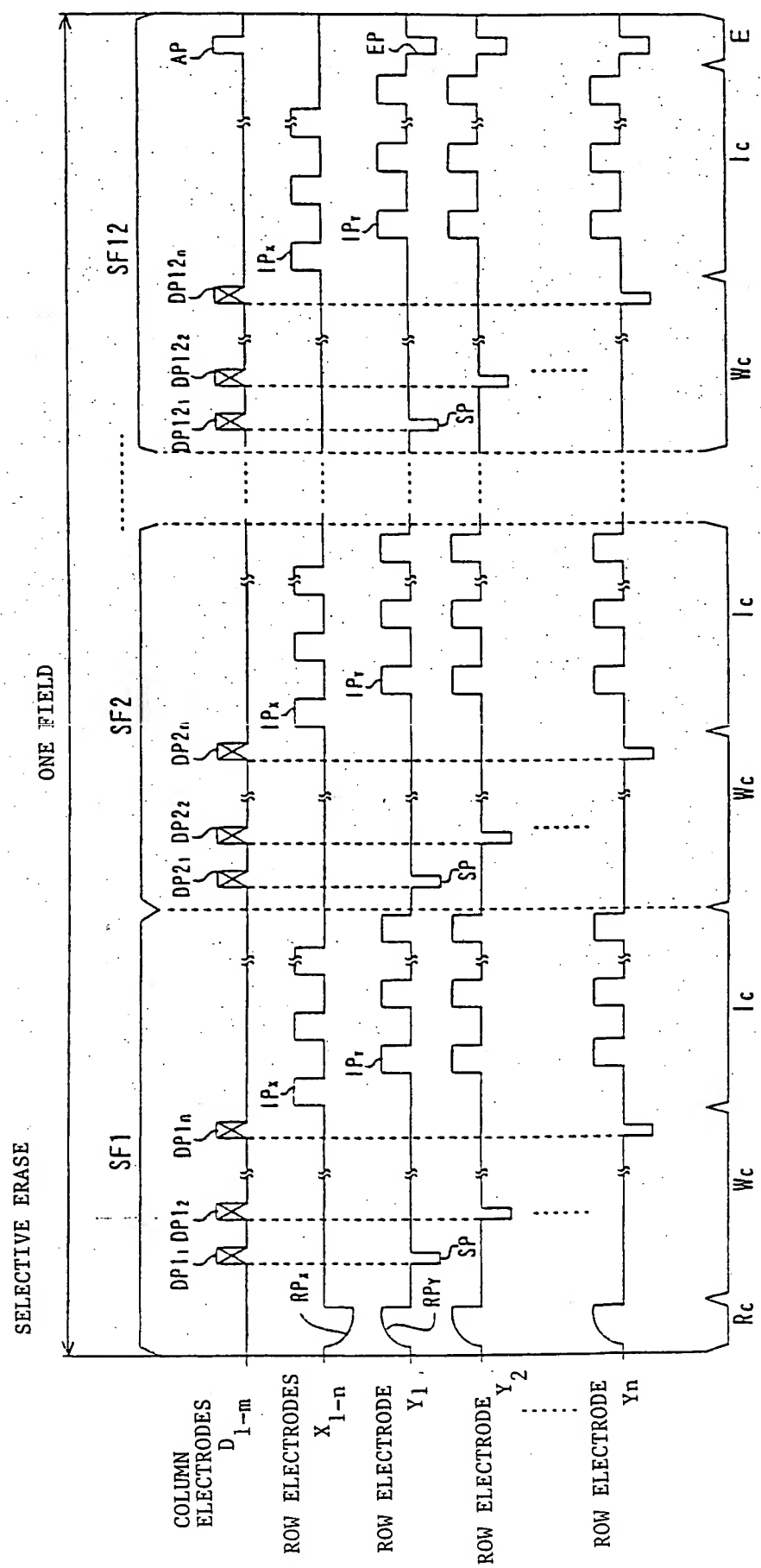


FIG. 4

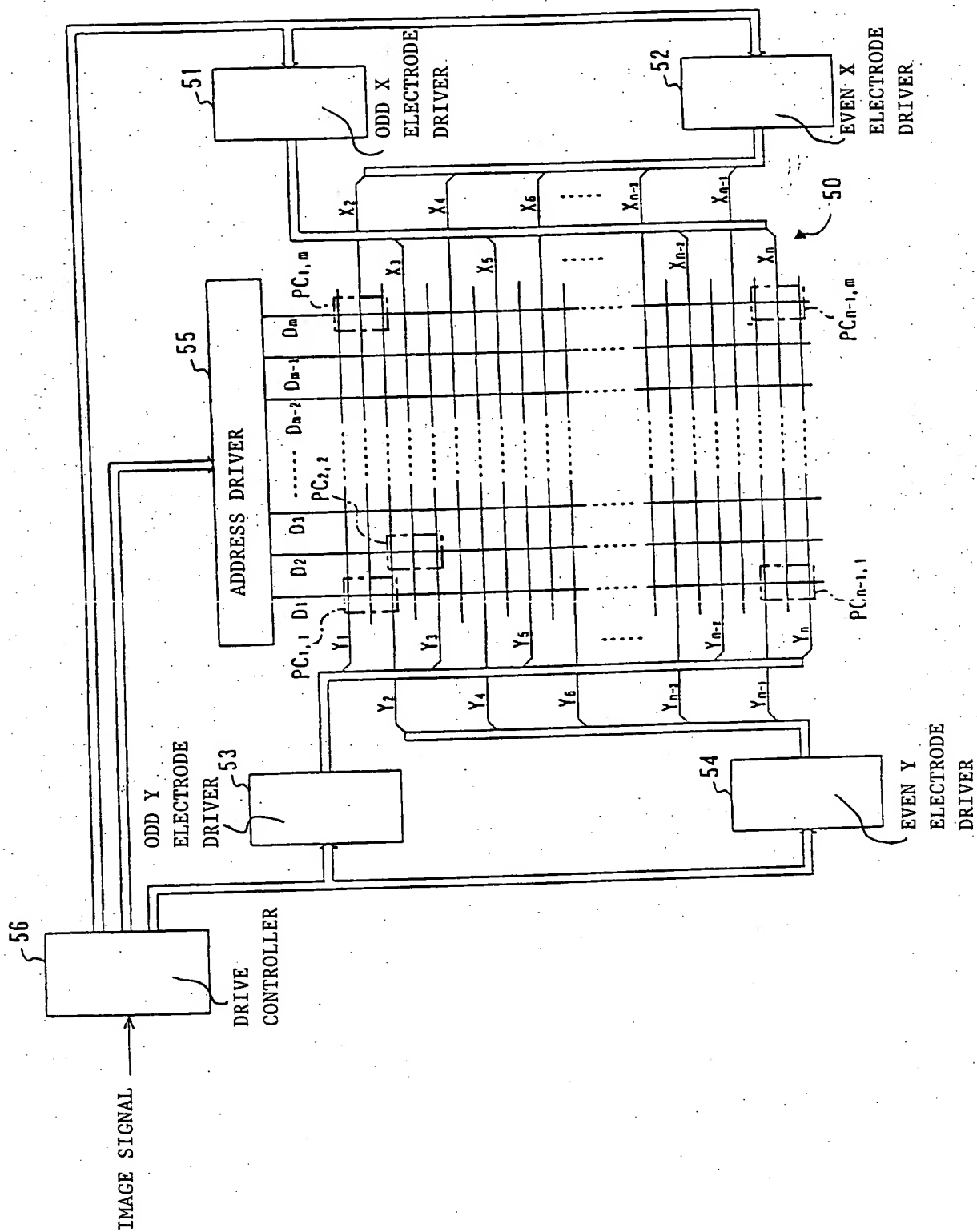


FIG. 5

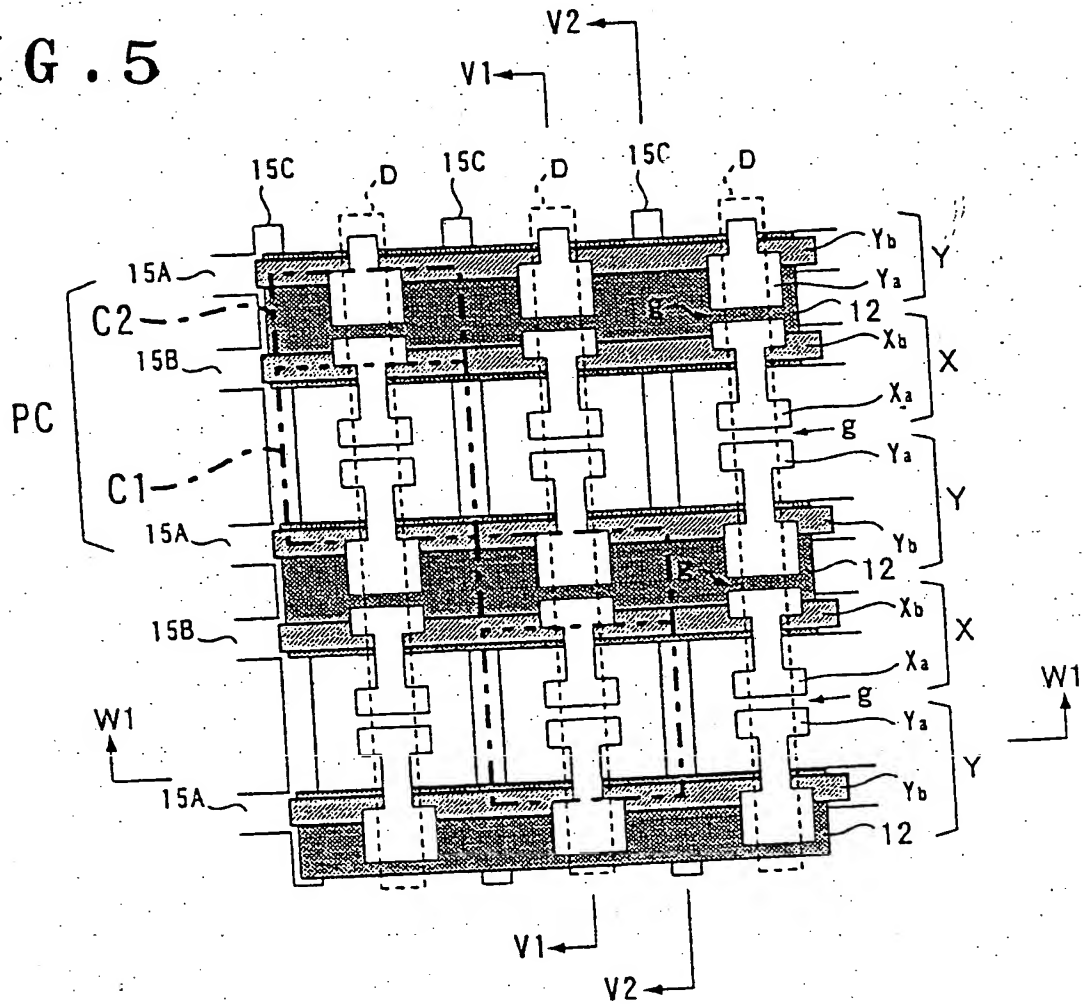
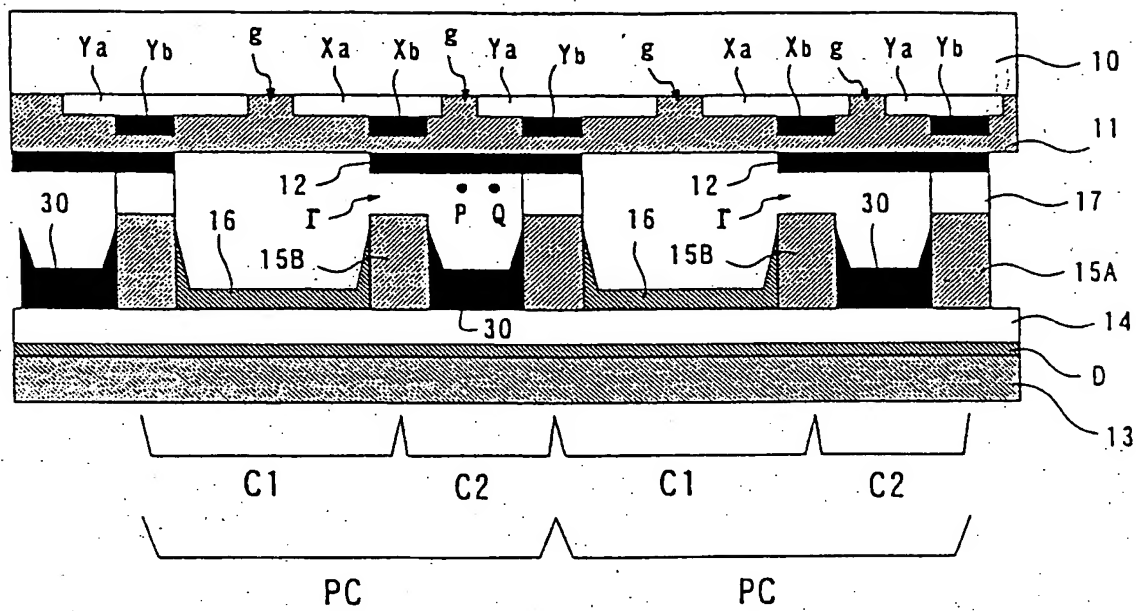


FIG. 6

V1-V1



V2-V2

FIG. 7

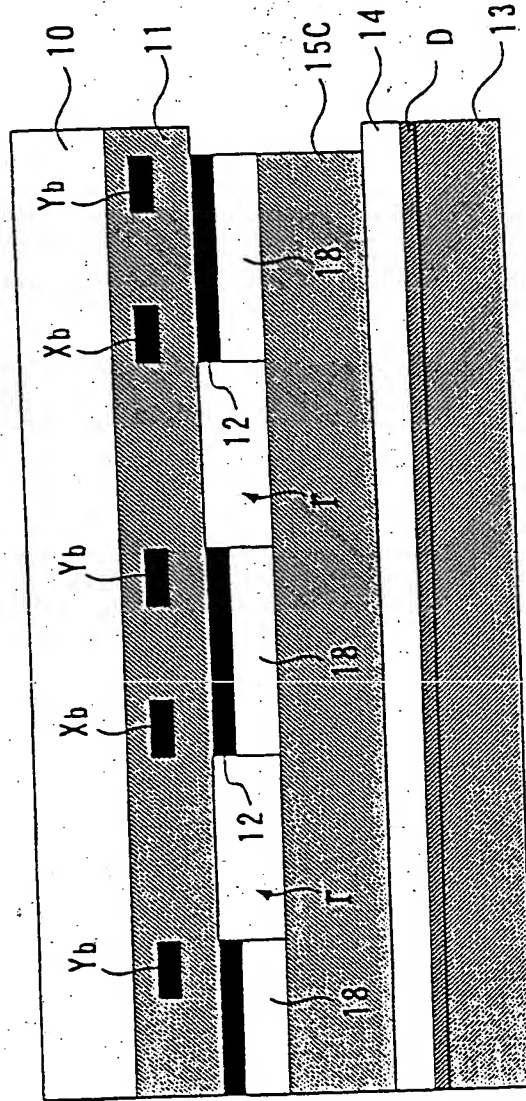


FIG. 8

W1-W1

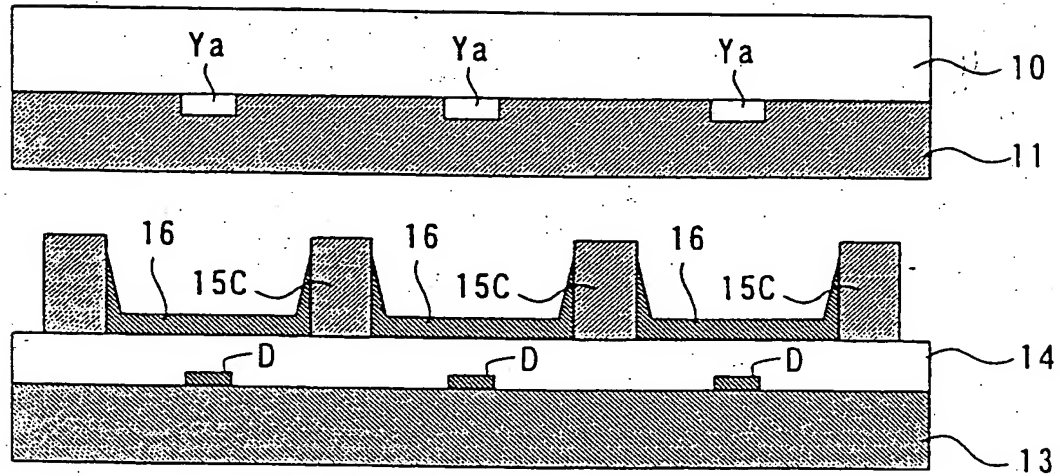


FIG. 9

GRADATION DRIVE	CONVERSION TABLE															LIGHT EMISSION PATTERN															
	PDS	GD															SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	SF 15
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15															
FIRST	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	◎														
SECOND	0001	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	◎														
THIRD	0010	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	◎	◎													
FOURTH	0011	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	◎	◎	◎												
FIFTH	0100	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	◎	◎	◎	◎											
SIXTH	0101	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	◎	◎	◎	◎	◎										
SEVENTH	0110	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	◎	◎	◎	◎	◎	◎									
EIGHTH	0111	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	◎	◎	◎	◎	◎	◎	◎								
NINTH	1000	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	◎	◎	◎	◎	◎	◎	◎	◎							
TENTH	1001	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	◎	◎	◎	◎	◎	◎	◎	◎	◎						
ELEVENTH	1010	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎					
TWELFTH	1011	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎				
THIRTEENTH	1100	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎			
FOURTEENTH	1101	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎		
FIFTEENTH	1110	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	
SIXTEENTH	1111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎

◎ : WRITING ADDRESS DISCHARGE + SUSUTAIN DISCHARGE
 LIGHT EMISSION

*: 0 OR 1

FIG. 10

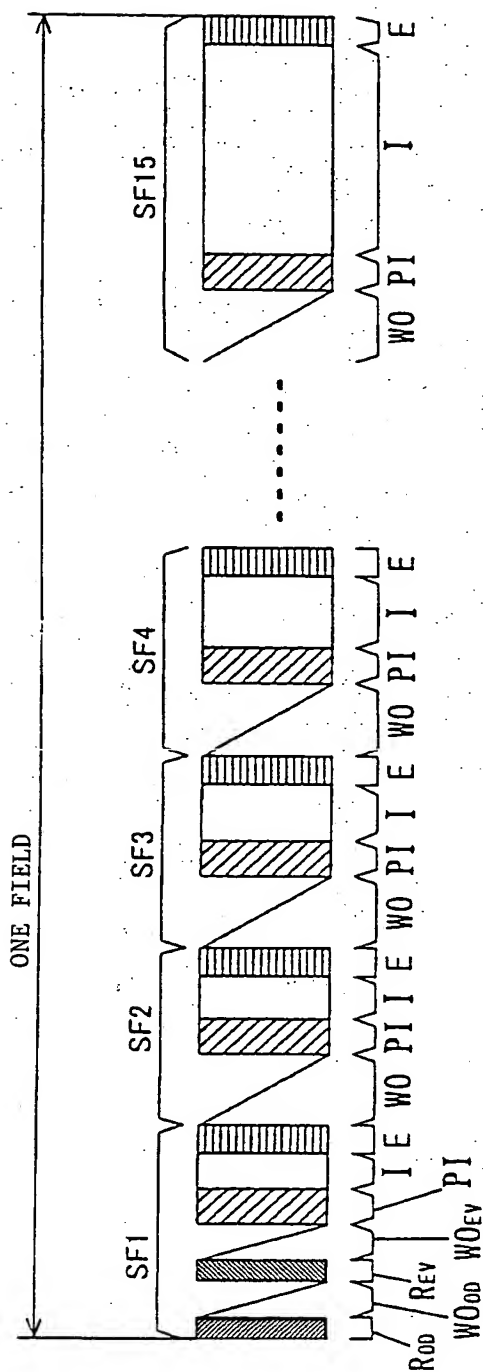


FIG. 12

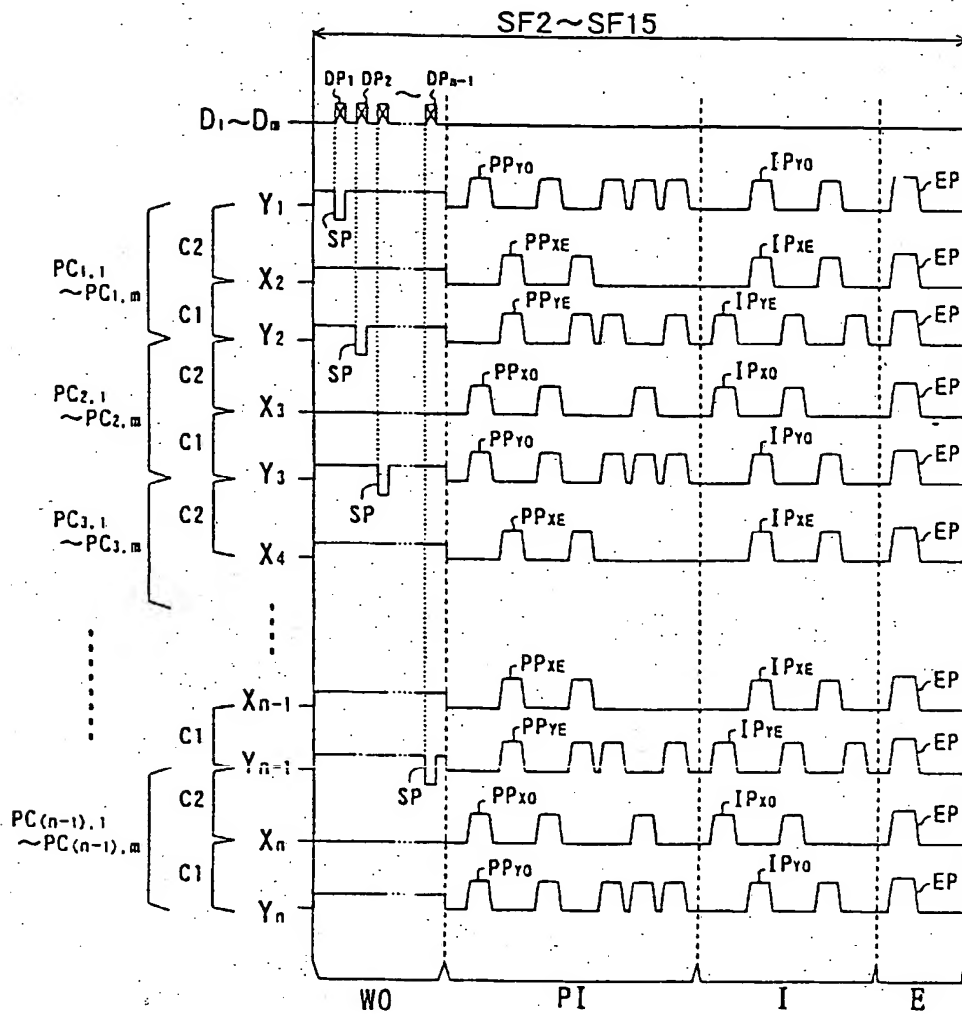
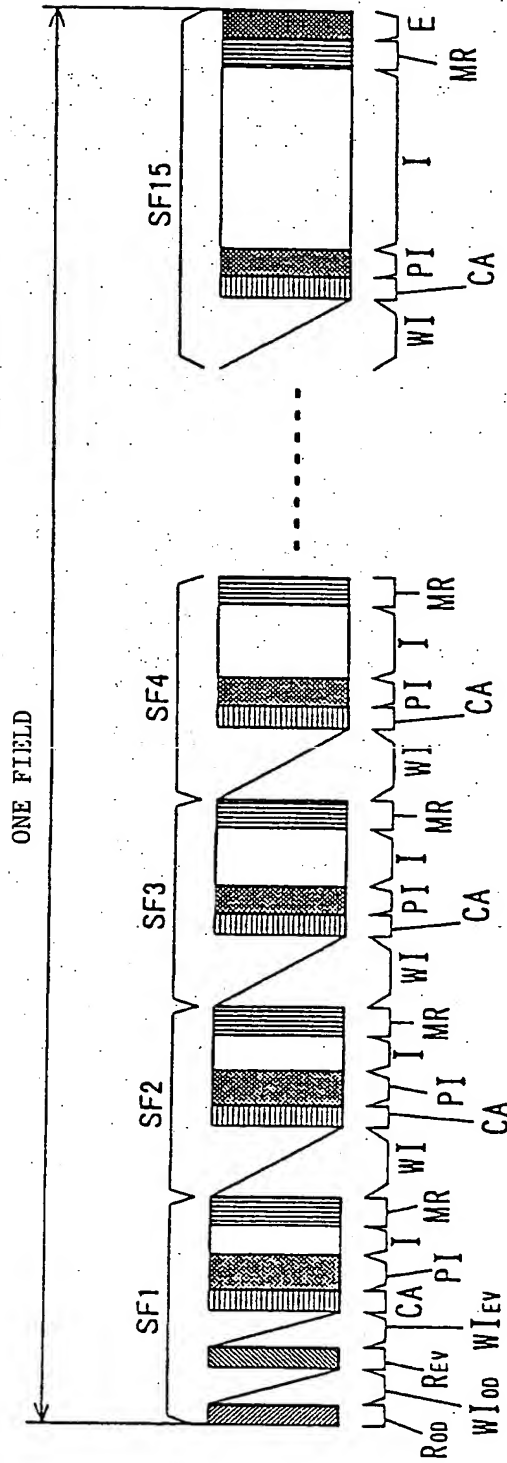


FIG. 13

GRADATION OPERATION	CONVERSION TABLE															LIGHT EMISSION PATTERN															
	PDS	GD															SF														
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIRST	0000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	●															
SECOND	0001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	○	●														
THIRD	0010	0	0	1	0	0	0	0	0	0	0	0	0	0	0	○	○	●													
FOURTH	0011	0	0	0	1	0	0	0	0	0	0	0	0	0	0	○	○	○	●												
FIFTH	0100	0	0	0	0	1	0	0	0	0	0	0	0	0	0	○	○	○	○	●											
SIXTH	0101	0	0	0	0	1	0	0	0	0	0	0	0	0	0	○	○	○	○	○	●										
SEVENTH	0110	0	0	0	0	0	1	0	0	0	0	0	0	0	0	○	○	○	○	○	○	●									
EIGHTH	0111	0	0	0	0	0	0	1	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	●							
NINTH	1000	0	0	0	0	0	0	0	1	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
TENTH	1001	0	0	0	0	0	0	0	0	1	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
ELEVENTH	1010	0	0	0	0	0	0	0	0	0	1	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
TWELFTH	1011	0	0	0	0	0	0	0	0	0	0	0	1	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
THIRTEENTH	1100	0	0	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
FOURTEENTH	1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
FIFTEENTH	1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
SIXTEENTH	1111	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○

●: ERASE ADDRESS DISCHARGE
 ○: SUSTAIN DISCHARGE LIGHT EMISSION

FIG. 14



The timing diagram illustrates the sequence of signals for the 7801 microcontroller across multiple cycles. The signals are grouped into four main sections: $PC_{1,1} \sim PC_{1,m}$, $PC_{2,1} \sim PC_{2,m}$, $PC_{3,1} \sim PC_{3,m}$, and $PC_{(n-1),1} \sim PC_{(n-1),m}$. Each section contains signals for RP_{12} , RP_{11} , SP , CP , PP_{1E} , IP_{1E} , and MP_{10} . The diagram also shows the $D_1 \sim D_n$ data bus and the $DP_1 DP_2 DP_{n-1}$ control signals. The signals are labeled with their respective pin numbers: RP_{12} (pin 12), RP_{11} (pin 11), SP (pin 10), CP (pin 9), PP_{1E} (pin 8), IP_{1E} (pin 7), and MP_{10} (pin 10).

~~TW01-03011~~

FIG. 16

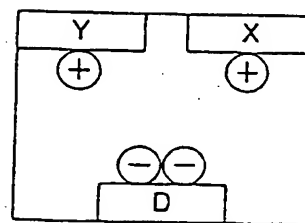
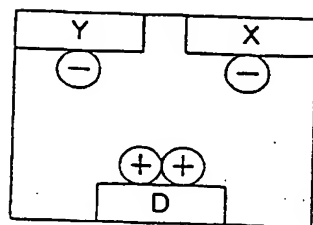
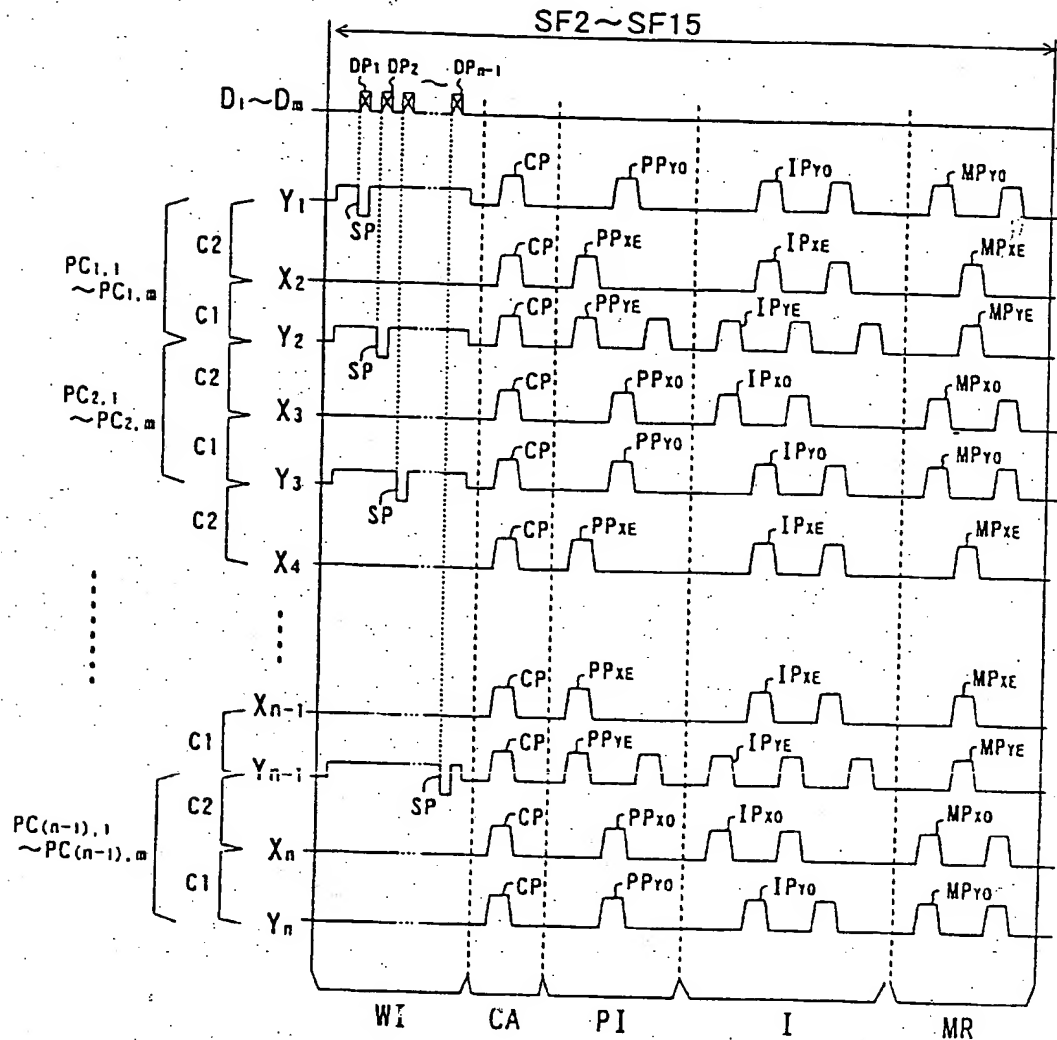


FIG. 17A

FIG. 17B